CLAIMS

1. A driving method for a liquid crystal display apparatus, including a substrate on which pixel electrodes and switching elements for on/off controlling voltage application to said pixel electrodes are arranged in matrix form; a substrate on which a counter electrode is provided; and a liquid crystal material having a spontaneous polarization sealed in a gap between said substrates, by applying a data voltage across said pixel electrodes and said counter electrode during an ON period of said switching elements and holding the data voltage during an OFF period so as to control a light transmission rate of said liquid crystal material which is determined by the data voltage,

wherein said driving method applies a reset voltage of a constant value in a first half period of said ON period, and applies said data voltage in a second half period of said ON period.

2. The driving method for the liquid crystal display apparatus as set forth in claim 1, wherein said first half period is substantially 1/2 of said ON period.

3. The driving method for the liquid crystal display apparatus as set forth in claim 1, wherein

said switching elements are on/off controlled at predetermined time intervals,

data voltages of opposite polarities are applied alternately in preceding and following ON periods, and

a reset voltage with a polarity opposite to the data voltage is applied in the same ON period.

4. The driving method for the liquid crystal display apparatus as set forth in claim 3, wherein said reset voltage is 0 V.

5. The driving method for the liquid crystal display apparatus as set forth in claim 3, wherein said first half period is substantially 1/2 of said ON period.

6. The driving method for the liquid crystal display apparatus as set forth in claim 5, wherein said reset voltage is 0 V.

7. A liquid crystal display apparatus including a substrate on which pixel electrodes and switching elements for on/off controlling voltage application to said pixel electrodes are arranged in matrix form; a substrate on which a counter electrode is provided; and a liquid crystal material having a spontaneous polarization sealed in a gap between said substrates, wherein a data voltage is applied across said pixel electrodes and said counter electrode during an ON period of said switching elements and the data voltage is held during an OFF period so as to control a light transmission rate of said liquid crystal material which is

determined by the data voltage, said liquid crystal display apparatus comprising:

means for applying a reset voltage of a predetermined value in a first half period of said ON period; and

means for applying said data voltage in a second half period of said ON period.

8. The liquid crystal display apparatus as set forth in claim 7, wherein

said switching elements are on/off controlled at predetermined time intervals,

said data voltage applied in an ON period has a polarity opposites to data voltages applied in ON periods preceding and following said ON period, and

said reset voltage has a polarity opposite to the data voltage in the same ON period.

9. The liquid crystal display apparatus as set forth in claim 8, wherein said first half period is substantially 1/2 of said ON period.

10. The liquid crystal display apparatus as set forth in claim 8, further comprising:

a first scanning line connected with the switching elements connected to pixels in odd-numbered matrix columns

among pixels in a matrix row, and a second scanning line connected with the switching elements connected to pixels in even-numbered matrix columns in the same matrix row; and

a scanning circuit having a plurality of output portions for on/off controlling said switching elements; wherein

said first scanning line and said second scanning line are alternately connected to the output portions of said scanning circuit.

11. The liquid crystal display apparatus as set forth in claim 10, further comprising a control circuit for controlling scanning of said scanning circuit, wherein

said scanning circuit comprises:

means for generating an operation clock signal for determining a scanning frequency of said scanning circuit; and

means for generating a scanning start signal, having a signal width equal to a two-clock period of said operation clock signal, for determining scanning start timing of said scanning circuit and said ON period.

12. The liquid crystal display apparatus as set forth in claim 7, wherein said first half period is substantially 1/2 of said ON period.

13. The liquid crystal display apparatus as set forth in claim 12, further comprising:

a first scanning line connected with the switching elements connected to pixels in odd-numbered matrix columns among pixels in a matrix row, and a second scanning line connected with the switching elements connected to pixels in even-numbered matrix columns in the same matrix row; and

a scanning circuit having a plurality of output portions for on/off controlling said switching elements; wherein

said first scanning line and said second scanning line are alternately connected to the output portions of said scanning circuit.

14. The liquid crystal display apparatus as set forth in claim 13, further comprising a control circuit for controlling scanning of said scanning circuit, wherein

said scanning circuit comprises:

means for generating an operation clock signal for determining a scanning frequency of said scanning circuit; and

means for generating a scanning start signal, having a signal width equal to a two-clock period of said operation clock signal, for determining scanning start timing of said scanning circuit and said ON period.

15. The liquid crystal display apparatus as set forth in claim 7, wherein said reset voltage is 0 V.

16. The liquid crystal display apparatus as set forth in

claim 15, further comprising:

a first scanning line connected with the switching elements connected to pixels in odd-numbered matrix columns among pixels in a matrix row, and a second scanning line connected with the switching elements connected to pixels in even-numbered matrix columns in the same matrix row; and

a scanning circuit having a plurality of output portions for on/off controlling said switching elements; wherein

said first scanning line and said second scanning line are alternately connected to the output portions of said scanning circuit.

17. The liquid crystal display apparatus as set forth in claim 16, further comprising a control circuit for controlling scanning of said scanning circuit, wherein

said scanning circuit comprises:

means for generating an operation clock signal for determining a scanning frequency of said scanning circuit; and

means for generating a scanning start signal, having a signal width equal to a two-clock period of said operation clock signal, for determining scanning start timing of said scanning circuit and said ON period.

18. The liquid crystal display apparatus as set forth in claim 7, further comprising:

a first scanning line connected with the switching

elements connected to pixels in odd-numbered matrix columns among pixels in a matrix row, and a second scanning line connected with the switching elements connected to pixels in even-numbered matrix columns in the same matrix row;

a first scanning circuit and second scanning circuit having a plurality of output portions for on/off controlling said switching elements; and

a control circuit for controlling scanning of said first scanning circuit and second scanning circuit; wherein

said first scanning line and second scanning line are connected to the output portions of said first scanning circuit and second scanning circuit, respectively, and

said control circuit comprises:

means for generating operation clock signals for determining scanning frequencies of said first scanning circuit and second scanning circuit so that polarities have a complementary relationship; and

means for generating a common scanning start signal for determining scanning start timing of said first scanning circuit and second scanning circuit and said ON period.

19. The liquid crystal display apparatus as set forth in claim 7, further comprising:

a first scanning line connected with the switching elements connected to pixels in odd-numbered matrix columns

among pixels in a matrix row, and a second scanning line connected with the switching elements connected to pixels in even-numbered matrix columns in the same matrix row; and

a scanning circuit having a plurality of output portions for on/off controlling said switching elements; wherein

said first scanning line and said second scanning line are alternately connected to the output portions of said scanning circuit.

20. The liquid crystal display apparatus as set forth in claim 19, further comprising a control circuit for controlling scanning of said scanning circuit, wherein

said scanning circuit comprises:

means for generating an operation clock signal for determining a scanning frequency of said scanning circuit; and

means for generating a scanning start signal, having a signal width equal to a two-clock period of said operation clock signal, for determining scanning start timing of said scanning circuit and said ON period.